CLAIMS

What is claimed is:

1. A method comprising:

receiving an input clock frequency and test data received at an input data frequency corresponding to the input clock frequency;

retaining a portion of the test data received in a first data buffer;

shifting the input clock frequency to an output clock frequency;

varying the output clock frequency over a period of time;

transmitting over the period of time, test data retained in the first data buffer, to a second data buffer of a chip that supports asynchronous communications, wherein transmitting occurs at an output data frequency corresponding to the output clock frequency.

2. The method of claim 1, wherein the output data frequency is a frequency of the test data retained in the first data buffer transmitted the output clock frequency.

3. The method of claim 1, wherein varying includes changing the output clock frequency every between 1,000 and 10,000 input clock frequency cycles.

4. The method of claim 1, wherein varying the output clock frequency includes:

setting the output clock frequency to greater than the input clock frequency while the test data retained in the first data buffer is greater than an upper watermark of an amount of test data to fill the second data buffer; and

setting the output clock frequency to less than the input clock frequency while the test data retained in the first data buffer is less than a lower watermark of an amount of test data to fill the second data buffer.

5. The method of claim 1, wherein varying includes increasing the output clock frequency to a selected maximum output data frequency during a first sub-period of the period of time and decreasing the output clock frequency to a selected minimum output data frequency during a second sub-period of the period of time.

6. The method of claim 1, wherein varying includes changing the output clock frequency during the period of time depending on at least one of a total duration of a test of the chip, the input data frequency, the output data frequency, the size of the retained portion of test data, and a duration between marker types of data packets included in the test data received.

7. The method of claim 6, wherein varying includes changing the output clock frequency by an amount to cause a size of the retained portion of test data to one of increase and decrease by a selected percent of a maximum data storage capacity of the first data buffer.

8. The method of claim 1, wherein varying the output clock frequency over the period of time includes one of increases and decreases the output clock frequency one of periodically for a selected period of time and for random intervals during the period of time.

9. The method of claim 1, wherein varying the output clock frequency over the period of time includes periodically increasing or decreasing the output clock frequency by one of a selected frequency and random increments of frequency.

10. The method of claim 9, wherein varying the output clock frequency includes setting the output clock frequency to a frequency sufficient to maintain the test data retained in the first data buffer between the upper watermark and the lower watermark.

11. The method of claim 1, wherein varying the output clock frequency over the period of time includes increasing and decreasing the output clock frequency in a range of between twenty percent greater and twenty percent less than the input clock frequency.

12. The method of claim 1, wherein varying the output data frequency over the period of time includes increasing and decreasing the output data frequency in a range of between ten percent greater and ten percent less than the input data frequency.

13. An apparatus comprising:

an elastic data buffer to receive test data at at least one input data frequency corresponding to at least one input clock frequency and to output the test data over a period of time at a plurality of output data frequencies corresponding to a plurality of output clock frequencies, the elastic data buffer having a maximum data storage capacity to retain a plurality of portions of the test data, a lower watermark of the maximum data storage capacity, and an upper watermark of the maximum data storage capacity;

a frequency modifier to shift the at least one input clock frequency to the plurality of output clock frequencies during the period of time, to increase the output clock frequency to a frequency greater than the input clock frequency when a portion of the test data retained is greater than the upper water mark, and to decrease the output clock frequency to a frequency less than the input clock frequency when a portion of the test data retained is less than the lower water mark.

14. The apparatus of claim 13, further comprising a transmitter to transmit the test data to be output during the period of time to a receive data buffer of a computing device that supports asynchronous communications.

15. The apparatus of claim 14, wherein the elastic data buffer has a maximum data storage capacity that is at least greater than a maximum data storage capacity of the receive data buffer.

16. The apparatus of claim 14, wherein the test data includes one of asynchronous communication data packets, marker type data packets, and data symbols having a selected number of bits of data to be interpreted by the chip.

17. The apparatus of claim 16, wherein the upper water mark is defined as the maximum data storage capacity minus at least the product of a selected integer and a data size of a data symbol; and the lower water mark is defined as at least the product of a selected integer and a data size of a data symbol.

18. The apparatus of claim 13, wherein the frequency modifier is to shift the at least one input clock frequency to the plurality of output clock frequencies during the period of time according to a test protocol.

19. The apparatus of claim 13, wherein the frequency modifier is to change the output clock frequency during the period of time by increments of between five percent and twenty five percent of the input clock frequency.

20. The apparatus of claim 19, wherein the increments are one of plus ten percent and minus ten percent of the input clock frequency.

21. A system comprising:

a digital signal processor that supports asynchronous communications across a link, the processor having a first elastic data buffer to receive data;

a test environment to provide a test frequency and test data to transmit to the first elastic data buffer at a first data frequency derived from the test frequency;

a frequency modifier to shift the test frequency to an output clock frequency and to vary the output clock frequency over a period of time;

a second elastic data buffer having a maximum data storage capacity larger than a maximum data storage capacity of the first elastic data buffer, the second elastic data buffer to retain a portion of the test data and to output the test data over the period of time to the first elastic data buffer at a second data frequency derived from the output clock frequency.

22. The system of claim 21, wherein the test environment comprises a test suite to generate the test frequency and an asynchronous communications link simulator to generate the test data.

23. The system of claim 21, wherein the second elastic data buffer has a maximum data storage capacity at least twice as large as a maximum data storage capacity of the first elastic data buffer.

24. An article of manufacture comprising:

a machine-readable medium having data therein which when accessed by a processor implements a test protocol, wherein the test protocol includes:

a) controlling an elastic data buffer to receive test data at at least one input data frequency corresponding to at least one input clock frequency and to output the test data over a period of time at a plurality of output data frequencies corresponding to a plurality of output clock frequencies, the elastic data buffer having a maximum data storage capacity to retain a plurality of portions of the test data, a lower watermark of the maximum data storage capacity, and an upper watermark of the maximum data storage capacity;

b) controlling a frequency modifier by causing the frequency modifier to shift the at least one input clock frequency to the plurality of output clock frequencies during the period of time, to increase the output clock frequency to a frequency greater than the input clock frequency when a portion of the test data retained is greater than the upper water mark, and to decrease the output clock frequency to a frequency less than the input clock frequency when a portion of the test data retained is less than the lower water mark.

25. The article of manufacture of claim 24, wherein the test protocol further causes a transmitter to transmit the test data retained in the elastic data buffer, over the period of time and at an output data frequency corresponding to the output clock frequency, to a second data buffer of a chip that supports asynchronous communications.

26. The article of manufacture of claim 24, wherein the test protocol further causes the frequency modifier to shift the output clock frequency prior to each of a plurality of sub-periods of the time period, wherein each sub-period is defined by the product of an integer greater than two and a duration between consecutive marker type data packets included in the test data to be received.

27. A system comprising:

a first chip having a first data buffer to receive data and a first data output to output data;

a second chip having a second data buffer to receive data and a second data output to output data;

a environment to provide a first clock frequency;

a first frequency modifier to shift the first clock frequency to a second clock frequency and to vary the second clock frequency over a period of time according to a test protocol;

a second frequency modifier to shift the first clock frequency to a third clock frequency and to vary the third clock frequency over a period of time according to the test protocol;

a first elastic data buffer to retain a portion of data output by the second data output and to output the data output by the second data output over the period of time to the first data buffer at a second data frequency corresponding to the second clock frequency; and

a second elastic data buffer to retain a portion of data output by the first data output and to output the data output by the first data output over the period of time to the second data buffer at a third data frequency corresponding to the third clock frequency.

28. The system of claim 27, wherein the first and second chips are digital communication chips and the test protocol tests whether the first and second data buffers are able to compensate for drift in data receive frequencies during an asynchronous communications test.

29. The system of claim 27, wherein the first and second data buffers are elastic data buffers that compensate for drift in data receive frequencies within specific allowed parameter ranges.